REMARKS

Claims 6-9 and 11-19 are pending in the present application. Replacement claim 6 has been presented herewith. Also, claims 16-19 have been presented herewith.

Information Disclosure Statement

Enclosed is a copy of an Information Disclosure Statement filed together with the present divisional application on January 25, 2001. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm on the record that the documents listed on the corresponding Information Disclosure Citation form PTO-A820 will be considered and cited of record in the present application.**

Claim Rejections-35 U.S.C. 102

Claims 11-14 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by the Seeds et al. reference (U.S. Patent No. 3,913,211). This rejection is respectfully traversed for the following reasons.

The Examiner has alleged that the Seeds et al. reference discloses all the features of claim 11 including "a connecting wire (21) coupled to the gate through the contact hole, the protective layer being formed on the field oxide only. (See Fig. 1h)". However, Applicant respectfully submits that the Seeds et al. reference as relied upon

by the Examiner does not disclose a protective layer formed on a field oxide only, as featured in claim 11.

As emphasized in the Amendment dated December 31, 2001, an object of the present application is to provide a protective layer over the field oxide, to prevent over etching of the field oxide and a resultant increase of inter-device leakage current as a result thereof. As described on pages 13 and 14 of the present application, oxide layer 36 as illustrated in Fig. 1(g) is deposited over the entire surface of the device, and thereafter etched anisotropically to form side walls 37, as illustrated in Fig. 1(h). Overetching is conducted in order to completely remove the oxide layer 36 formed on gate 35 and silicon substrate 31. As specifically described on page 14, lines 1-4 of the application, field oxide layer 34 is protected by polysilicon layer 12, so that overetching of field oxide layer 36 is prevented. As described on page 13, lines 2-3 of the application, **polysilicon layer 12 as the protective layer is formed only on the field oxide layer 34, as illustrated in Fig. 1(f).**

Applicant respectfully submits that the Seeds et al. reference does not include a protective layer that is formed on a field oxide only, as featured in claim 11. Particularly, polycrystalline silicon layer 17d as illustrated in Fig. 1h of the Seeds et al. reference is formed on field oxide 16a **and on source/drain region 19a.** As specifically described in column 4, lines 51-59 of the Seeds et al. reference, polycrystalline silicon layer 17d overlies not only part of the active region of the device but also part of the field of the device. Thus, polycrystalline silicon layer 17d of the

Seeds et al. reference cannot be interpreted as the protective layer of claim 11, because polycrystalline silicon layer 17d is not "formed on said field oxide only", but is also formed on an active region of the device.

Also, Applicant respectfully submits that polycrystalline silicon layer 17d of the Seeds et al. reference is not a protective layer. As described in column 4, lines 51-59 of the Seeds et al. reference, polycrystalline silicon layer 17d is doped to serve as a conductive lead to the active region formed in substrate 11 beneath opening 12b in gate oxide 12. Polycrystalline silicon layer 17d is not described as providing protection. In contrast, as described in column 6, lines 9-14 of the Seeds et al. reference, gate oxide 12 protects the surface of substrate 11 on which the transistors are formed during processing, to thereby prevent impurities from reaching the interface between oxide 12 and substrate 11.

Accordingly, Applicant respectfully submits that the semiconductor device of claim 11 distinguishes over the Seeds et al. reference as relied upon by the Examiner, and that this rejection of claims 11-14 is improper for at least the above reasons. **If this rejection is to be maintained, the Examiner is respectfully requested to establish on the record how polycrystalline silicon layer 17d of the Seeds et al. reference may be interpreted as "being formed on said field oxide only", and how polycrystalline silicon layer 17d may be interpreted as a protective layer.**

Claims 6-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Seeds et al. reference, in view of the Tomijima et al. reference (Japanese

Patent Publication No. 2-260639). This rejection, insofar as it may pertain to the presently pending claims is traversed in view of the following.

The semiconductor device of claim 6 includes in combination first and second gates "formed on active regions of a substrate, said first and second gates each consisting of a refractory metal layer on a polysilicon layer"; side walls "formed on side surfaces of said first and second gates, said side walls being a silicon oxide film", and a protective layer "formed on said field oxide, said protective layer being a material different than said field oxide". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

As emphasized previously, the protective layer of the present application prevents overetching of the field oxide, during formation of gate side walls. As noted, polycrystalline silicon layer 17d of the Seeds et al. reference is a conductive lead to the active region formed in substrate 11, as illustrated in Figs. 1e and 1f. Polycrystalline silicon layer 17d of the Seeds et al. reference is not a protective layer. Also, contrary to the Examiner's position, the Seeds et al. reference does not include side walls formed on a gate, and particularly side walls that are a silicon oxide film. The prior art as relied upon by the Examiner also fails to disclose or make obvious first and second gates each consisting of a refractory metal layer on a polysilicon layer.

Accordingly, Applicant respectfully submits that the semiconductor device of claim 6 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 6-9 is improper for at least these reasons. Applicant also respectfully submits that the prior art as relied

upon by the Examiner does not disclose or even remotely suggest a protective layer "formed on said field oxide only", as featured in claim 8.

Claim 15 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Seeds et al. reference, in further view of the Tomijima et al. reference. Applicant respectfully submits that claim 15 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least the reasons as set forth above with respect to claim 11.

Claims 16-19

Applicant respectfully submits that the semiconductor device of claim 16 distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner, for at least similar reasons as set forth above. Particularly, the prior art as relied upon by the Examiner does not disclose or suggest a protective layer formed on a field oxide only, a gate consisting of a refractory metal layer on a polysilicon layer, and side walls that are silicon oxide film on side surfaces of a gate. Accordingly, Applicant respectfully submits that claims 16-19 are allowable over the relied upon prior art for at least the above reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for

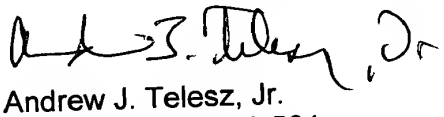
at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



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Enclosures: Version with marked-up changes
Copy of Information Disclosure Statement and PTO-A820 form dated January 25, 2001

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Claims:

6. (Twice Amended) A semiconductor device comprising:

first and second gates formed on active regions of a substrate, said first and second gates each consisting of a refractory metal layer on a polysilicon layer;

a field oxide formed on the substrate between said first and second gates;

side walls formed on side surfaces of said first and second gates, said side walls being a silicon oxide film;

a protective layer formed on said field oxide, said protective layer being a material different than said field oxide;

an insulating layer formed on the substrate, [including] said first and second gates, said side walls, said field oxide and said protective layer;

a contact hole formed through said insulating layer; and

a connecting wire coupled to said gate through said contact hole.